Lab 5 (2nd Session)

Verilog Basics

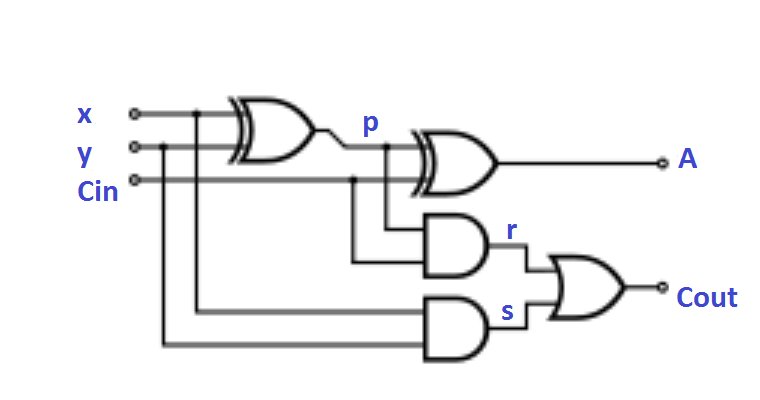
Continuous Assignment

* In-Lab

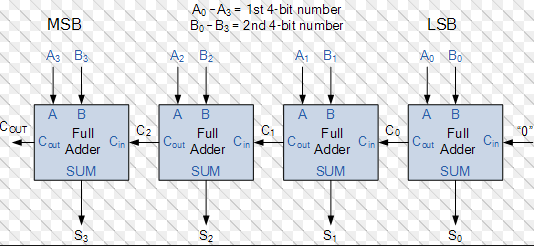
Bring previous codes (D-Flipflop) with you.

**Task (Use Vectors for declaring variables)**

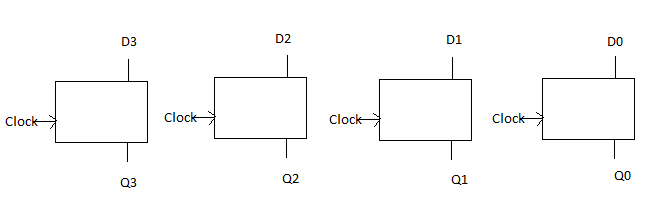
* **Write Verilog code for a 4-bit adder using four full adders**



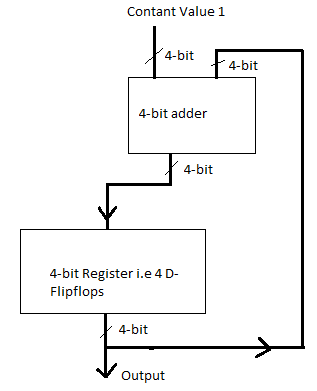
**Full Adder**

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* **Write Verilog HDL description for a 4-bit register with parallel load using D-Flipflops.**

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* Post-Lab
* **Write a Verilog HDL description for 4-bit counter using previous two task.**

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* **Use Univeral Shift Register to create a 4 bit counter.**
* **Your lab report, a .doc file, should contain properly commented Post-Lab task code, with Screenshots(of print preview) of Schematic and waveforms, and Critical Analysis.**
* **The report must have a title page in the pescribed format.**
* **Name the .doc file RegNo.docx; eg SP14-BCE-99.docx**
* **Send it to** [**khiyamiftikhar@gmail.com**](mailto:khiyamiftikhar@gmail.com)**. With subject Lab No.**